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PATENT
Dkt. STL10986

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Sundeep Chauhan**
Assignee: **SEAGATE TECHNOLOGY LLC**
Application No.: **10/625,386** Art Unit: **2816**
Filed: **July 23, 2003** Examiner: **Hai L. Nguyen**
For: **HIGH SPEED DIGITAL PHASE/FREQUENCY COMPARATOR FOR PHASE LOCKED LOOPS**

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ATTENTION: Board of Patent Appeals and Interferences

APPELLANT'S BRIEF

Appellant's Brief is in furtherance of the Notice of Appeal filed September 17, 2007.

This brief contains these items under the following headings, and in the order set forth below:

I. REAL PARTY IN INTEREST

The real party in interest in this Appeal is Seagate Technology LLC.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this Appeal.

III. STATUS OF CLAIMS

The status of the claims in this application is:

Claim	Status
1. (Previously presented)	Independent.
2. (Previously presented)	Depends from claim 7.
3. (Previously presented)	Depends from claim 2.
4. (Previously presented)	Depends from claim 3.
5. (Previously presented)	Depends from claim 4.
6. (Previously presented)	Depends from claim 4.
7. (Previously presented)	Depends from claim 1.
8. (Previously presented)	Depends from claim 1.
9. (Previously presented)	Depends from claim 1.
10. (Previously presented)	Independent.
11. (Original)	Depends from claim 10.
12. (Original)	Depends from claim 11.
13. (Original)	Depends from claim 12.
14. (Original)	Depends from claim 13.
15. (Original)	Depends from claim 13.
16. (Original)	Depends from claim 10.
17. (Original)	Depends from claim 10.
18. (Previously presented)	Depends from claim 10.
19. (Previously presented)	Depends from claim 10.
20. (Previously presented)	Independent.
21. (Original)	Depends from claim 20.
22. (Original)	Depends from claim 21.
23. (Original)	Depends from claim 20.
24. (Original)	Depends from claim 23.
25. (Original)	Depends from claim 20.
26. (Original)	Depends from claim 25.

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application: 1-26.

B. STATUS OF ALL THE CLAIMS

1. Claims canceled: none
2. Claims withdrawn from consideration but not canceled: none
3. Claims pending: 1-26
4. Claims allowed: none
5. Claims rejected: 1-3, 7-12, 16-22, 25, and 26
6. Claims objected to: 4-6, 13-15, 23, and 24

C. CLAIMS ON APPEAL

Claims now on appeal: 1-3, 7-12, 16-22, 25, and 26

IV. STATUS OF AMENDMENTS

This is Appellant's second appeal brief in this case. The Office reopened prosecution in response to Appellant's first appeal brief filed May 16, 2005. In reply to the final rejection of February 28, 2006 Appellant filed a Pre-Brief Request for Review on June 28, 2006. The Panel's Decision of August 30, 2006 was to again reopen prosecution. The two subsequent Office actions of November 14, 2006 and May 17, 2007 maintained the rejections on the same basis. Appellant filed a second Pre-Brief Request for Review on September 17, 2007. This Appeal Brief is in response to the Panel's Decision of October 22, 2007to proceed to appeal on the merits.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 features a phase/frequency comparator that generates a phase error responsive to a transition location signal. This is disclosed in the specification at least at page 7 lines 1-23:

> N-bit parallel latch 302 latches in the outputs of N-bit tapped delay line 300 when reference clock signal 303 transitions (either from low to high or high to low, depending on the latch design). The output of N-bit parallel latch 302 is thus a snapshot of the progress of input signal 301 through N-bit tapped delay line 300 over one cycle of reference clock signal 303. This snapshot is fed into N-bit edge detect circuit 304, which is described in more detail in FIG. 4. N-bit edge detect circuit 304 outputs a single bit at the transition point of a falling edge (or rising edge, depending on the design) in the snapshot provided by N-bit parallel latch 302. This signal bit may be referred to as a transition location signal.

> Weighted encoder 306 converts the output of N-bit edge-detect circuit 304 into a numerical phase difference value that reflects the phase difference between input signal 301 and reference signal 303. Phase difference calculator 308 calculates the difference between the output of weighted encoder 306 and a lock point input 309. Lock point input 309 is used to specify a particular desired phase difference between input signal 301 and reference signal 303. The output of phase difference calculator 308 is added to the value stored in an accumulator 310. Accumulator 310 serves as the digital counterpart to low-pass filter 108 in the analog PLL of FIG. 1, as an accumulator in digital signal processing acts like an integrator (which is a kind of low-pass filter) in analog signal processing. The resulting output 311 is a digital phase error signal that can be used to control a numerically controlled oscillator (NCO), as depicted in FIG. 7.

Claim 10 features a controllable oscillator (DDS 704 in FIG. 7) and a phase/frequency comparator (ADPFC 700 in FIG. 7). The phase/frequency comparator is coupled to the controllable oscillator such than an output of the controllable oscillator is connected in a feedback loop to an input of the phase/frequency comparator and an output of the phase/frequency comparator is connected through a forward path to a control input of the controlled oscillator. Disclosure for this is found at least in the specification at least at page 10 lines 3-19.

The phase/frequency comparator includes a phase detecting stage, encoding circuitry coupled to the phase detecting stage and an accumulator coupled to the encoding circuitry. This is disclosed in the specification at least at page 6 line 11 to page 7 line 23.

Claim 20 features generating a snapshot of a first signal in response to receiving a second signal and mapping the snapshot to a numerical phase difference value that is generated responsive to a signal that corresponds to a transition location of the first signal.

These features are also disclosed in the specification at least at page 6 line 11 to page 7 line 23.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3, 7, 10-12, 16, 17, 20-22, 25, and 26 stand rejected under 35 USC 102 as being anticipated by U.S. 6,429,693 to Staszewski ("Staszewski '693").

VII. ARGUMENT

THE REJECTION OF INDEPENDENT CLAIMS 1 AND 20 IS REVERSIBLE ERROR BECAUSE THE OFFICE HAS FAILED TO SUBSTANTIATE A LEGAL BASIS WHY APPELLANT IS NOT ENTITLED TO THE CLAIMED SUBJECT MATTER IN TERMS OF THE *TRANSISTION LOCATION SIGNAL* RECITED BY THOSE CLAIMS

1. The Office admits the *transition location signal* is patentable.

Independent claims 1 and 20 recite the following in pertinent part:

> *a phase/frequency comparator circuit that is configured to generate a phase error responsive to a transition location signal.*
> (excerpt of claim 1, emphasis added)

> *mapping the snapshot to a numerical phase difference value that is generated responsive to a signal that corresponds to a transition location of the first signal.*
> *(excerpt of claim 20, emphasis added)*

The Office recognizes the patentability of the *transition location signal* in terms of the more particular language of claims depending from the independent claims 1 and 20:

> The prior art of record fails to disclose or fairly suggest a phase/frequency comparator (as shown in Fig. 3)...having specific limitations such as an encoding circuitry includes [sic] an edge detector (304) coupled to the parallel latch (300, 302)...wherein the edge detector outputs a transition location signal....

(Office Action of 5/17/07 ppg. 7-8, emphasis added)[1]

Therefore, the issue on appeal is not whether the *transition location signal* is patentable, but rather whether Appellant is entitled to the subject matter expressed in terms of the language "transition location signal" itself.

2. The broadest reasonable construction of *transition location signal* is its ordinary meaning.

During examination claims are given their "broadest reasonable interpretation consistent with the specification."[2] The "broadest reasonable interpretation" is the meaning that the skilled artisan would give to the claim term in view of the associated usage provided in the specification.[3] A construction that is inconsistent with the written description would not be arrived at by the skilled artisan, and is therefore not a "reasonable interpretation."[4]

The Office is obligated not to supplant the ordinary, simple English meaning of words in a claim when that ordinary meaning is clear and unquestionable; in other words, when the words mean exactly what they say.[5] Here, Appellant has pointed out that the phrase *transition location signal* ordinarily means a signal that indicates a transition location.[6] In the Office's explanation for allowable subject matter (excerpted above), the Office acknowledges that the edge detector (304) in the embodiments of FIG. 3 outputs a signal that indicates a transition location.

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[1] See also Office Action of 11/14/2006 pg. 7; Office Action of 5/28/2006 ppg. 8-9; Office Action of 7/28/2005 pg. 8.
[2] *Phillips v. AWH Corp.*, 75 USPQ2d 1321 (Fed. Cir. 2005)(en Banc); MPEP 2111
[3] *In re American Academy of Science Technical Center*, 70 USPQ2d 1827 (Fed. Cir. 2004); *In re Cortright*, 49 USPQ2d 1463, 1468 (Fed. Cir. 1999); *In re Morris*, 44 USPQ2d 1023 (Fed. Cir. 1997)
[4] *Phillips, supra*; *In re Morris, supra*; *In re Zletz*, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)
[5] *Chef America v. Lamb-Weston*, 358 F.3d 1371, 1373 (Fed. Cir. 2004)
[6] Appellant's Pre-Brief Request of 9/17/2007 pg. 2; Appellant's Response of 8/17/2007 pg. 10

Appellant has shown that the ordinary meaning of *transition location signal* is consistent with the explicit definition found in the specification: [7]

> N-bit edge detect circuit 304 outputs a single bit at the transition point of a falling edge (or rising edge, depending on the design) in the snapshot provided by N-bit parallel latch 302. This signal bit may be referred to as a transition location signal.
> (specification pg. 7 lines 7-10, emphasis added)

"During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow. When the applicant states the meaning that the claim terms are intended to have, the claims are examined with that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art."[8] Here, Appellant has unquestionably made it explicitly clear what the intended meaning of *transition location signal* is, and the Office is obligated to consider the disputed term in the context of that meaning.

One position taken by the Office is that this explicit definition provided by the specification is insufficient to define a special meaning for *transition location signal* because the permissive word "may" is used.[9] That reasoning is irrelevant on the merits because Appellant agrees that the ordinary meaning of the disputed phrase, consistent with its usage in the specification, is controlling. There is no need for the Board to ascertain whether any special meaning for the disputed term is defined by the specification.

3. The Office has failed to substantiate anticipation of claims 1 and 20 by not showing evidence that Staszewski '693 discloses a *transition location signal.*

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[7] Appellant's Pre-Brief Request of 9/17/2007 pg. 2; Appellant's Response of 8/17/2007 pg. 10; Appellant's Pre-Brief Request of 6/28/2006 pg. 2; Appellant's Response of 5/30/2006 pg. 10; Appellant's Response of 11/28/2005 pg. 14; Appellant's Brief of 5/16/2005 pg. 8; Appellant's Response of 2/15/2005 pg. 10.
[8] *In re Alex Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)
[9] Office Action of 11/14/2006 pg. 6 line 18 to pg. 7 line 4; Office Action of 5/28/2006 pg. 6 line 14 to pg. 7 line 14.

Disclosed embodiments of a signal that indicates a transition location include the signal comparator structure employing an N-bit delay line 300 receiving CLOCK1 signal and an N-bit parallel latch 302 receiving CLOCK2 signal:

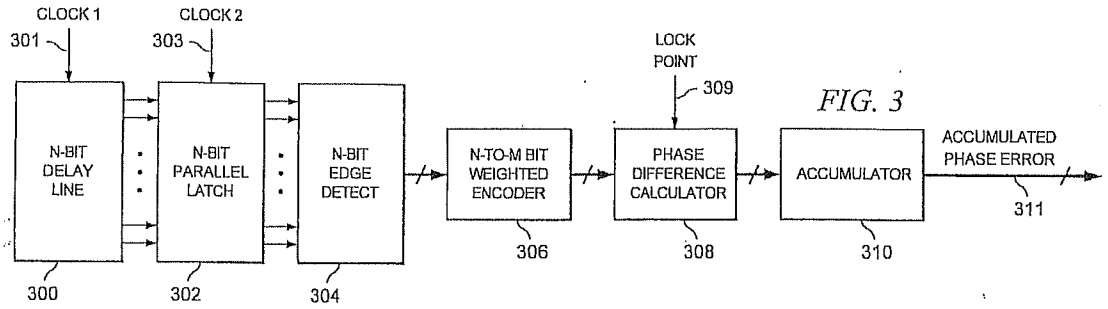


FIG. 3

The N-bit delay line 300 is reset each time a transition occurs in CLOCK1.[10] The CLOCK1 transition propagates through the N-bit line 300, the status of the propagation being instantaneously observable via the respective N outputs.[11] When CLOCK2 transitions, then the N-bit parallel latch 302 captures a snapshot of the N outputs.[12] That snapshot captures the progress of the CLOCK1 transition as it propagates through the N-bit delay line 300.[13] Thus, the N-bit edge detect 304 outputs a single bit at the CLOCK1 transition; that signal indicating the transition location of the CLOCK1 transition.

The final rejection of claims 1 and 20 is based on the Office's rationale that the snapshot signal 604 of the plurality of registers 504 in Staszewski '693 anticipates the claimed *transition location signal*:

> Thus, by given the broadest reasonable interpretation, TDC_RISE, TDC_FALL is the transition location signal, since the snapshot taken by the parallel latches (504's in Fig. 5 of Staszewski) directly indicates the location of the feedback clock 114 through the tapped delay line 502's

[10] Specification pg. 6 lines 23-26.
[11] Specification pg. 6 lines 12-23.
[12] Specification pg. 7 lines 1-3.
[13] Specification pg. 7 lines 3-6.

precisely at the occurrence of the feedback transition signal 110.
(Office Action of 2/28/2006, cited in final rejection of 5/17/2007, emphasis added)

However, Staszewski '693 itself clearly defines the snapshot 604 to be a timing signal, not a location signal as claimed:

During a positive transition (enumerated 602 in FIG. 6) of the reference clock FREF 110, each of the latch/registers 504 will be queried in order to obtain a snapshot of the quantized fractional phase difference between the dVCO 104 clock signal CKV 114 phase and the reference clock FREF 110 signal phase.
(Staszewski '693 col. 8 lines 30-36, emphasis added)

During a positive transition 602 of the reference oscillator FREF 110, the plurality of latch/registers 504 are accessed to obtain a snapshot 604 of the delayed replicas of the dVCO clock CKV 114 relative to the rising edge of the reference oscillator FREF 110. The snapshot 604 can be seen to express the time difference as a digital word.
(Staszewski '693, col. 8 lines 45-46)

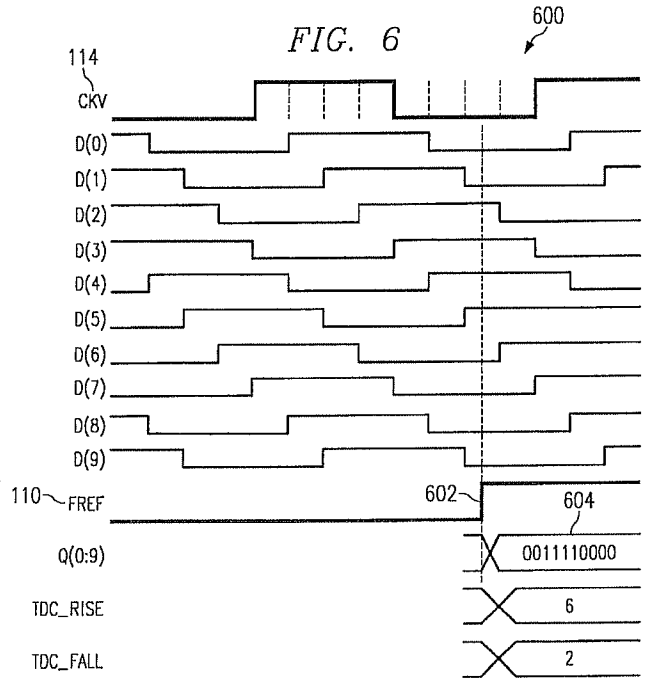
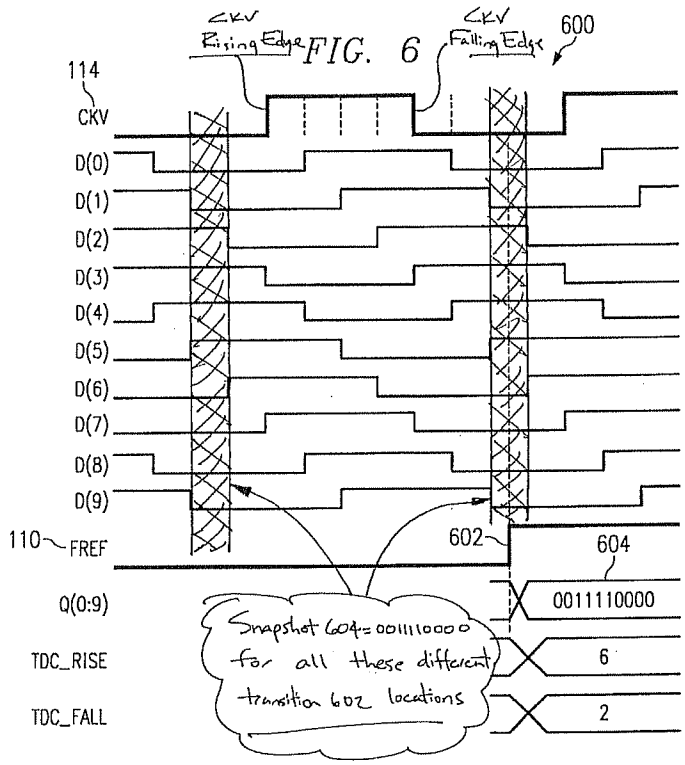


FIG. 6 of Staszewski '693 clearly defines the snapshot signal 604 as a multi-bit word, each bit being associated with the state of a respective delayed replica D(n) of the oscillator 104 (dVCO) pulse CKV 114. The skilled artisan readily recognizes that the snapshot signal 604 indicates a timing difference between the FREF transition 602 and the CKV 114, not a location of FREF transition 602.

The skilled artisan readily understands that the snapshot signal 604 cannot define the location of the FREF transition 602 because Staszewski '693 does not synchronize any reference between an edge (rising or falling) of CKV 114 with respect to the FREF transition 602. Rather, the snapshot signal 604 is an observation of an instantaneous state within a continuum of consecutively delayed CKV 114 replica pulses D(0), D(1), D(2)....

Appellant has shown that the snapshot signal 604 is irrespective of FREF transition 602 location because there are a plurality of different locations that the FREF transition 602 could occur and yet be associated with the same snapshot signal 604.[14] For example, the following marked-up FIG. 6 of Staszewski '693 has been shown to illustrate that the snapshot signal 604 cannot differentiate between whether the FREF transition 602 is leading or lagging the CKV 114, in that the same snapshot signal 604 is associated both with multiple locations prior to the CKV rising edge and at multiple locations following the CKV falling edge:

[14] Appellant's Pre-Brief Request of 9/17/2007 pg. 4; Appellant's Response of 8/17/2007 pg. 13; Appellant's Response of 2/14/2007 pg. 10.



The skilled artisan readily understands that Staszewski '693 discloses employing the snapshot signal 604 to determine a timing difference between FREF and CKV, and then compensates for the phase difference in a manner described by equations 8-13.[15] The skilled artisan also readily appreciates the substantive distinction between the timing difference disclosed by Staszewski '693 and the *transition location signal* of the claimed embodiments.

The final position taken by the Office, in response to Appellant's evidence that Staszewski's snapshot signal 604 indicates multiple locations, is that:

> However, Examiner respectfully disagrees because nothing in the claim recited that the transition locations of the transition location signal must not be the same. Furthermore, the skilled artisan in the art would clearly understand that a transition location signal as the signal that corresponds to transition location of the signal FREF (110)

[15] Staszewski '693 col. 8 lines 50-55.

> makes its transition at each of the locations requiring the signal FREF as depicted in FIG. 6 of Staszewski et al. (Office Action of 5/17/2007 pg. 6 para. 7)

Appellant respectfully traverses that rationale as being erroneous on many fronts. First, in the former portion the Office asserts that *transition location signal* reasonably means "transition locations signal." That reasoning is entirely contrary to the ordinary meaning of the singular form of the noun "location," and contrary to the disclosure that the N-bit edge detect circuit 304 outputs a single bit defining the transition location signal.[16] The broadest reasonable meaning of the disputed claim language consistent with its usage in the specification precludes the *transition location signal* from meaning a signal that indicates multiple transition locations.

Second, in the latter portion the Office asserts that the skilled artisan would believe that FREF 110 in Staszewski '693 makes its transition 602 at all the multiple locations associated with the same snapshot signal 604. That reasoning is a mischaracterization of what Staszewski '693 actually discloses. Appellant has shown that Staszewski '693 uses the time difference expressed by the snapshot signal 604 as input to the frequency synthesizer 100 to compensate for phase differences via the computations set forth in equations. 8-13.[17] The Office's assertion that the common snapshot signal 604 of 0011110000 (in FIG. 6 of Staszewski '693) is meaningful as a "transition location signal" at all the locations depicted in Appellant's marked up FIG. 6 above, both before the CKV rising edge and after the CKV falling edge, necessarily requires that the subsequent computations set forth in equations 8-13 of Staszewski '693 must be superfluous. Appellant respectfully disagrees that the skilled artisan would reach that conclusion asserted by the Office.

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[16] Specification pg. 7 lines 7-10.
[17] Appellant's Pre-Brief Request of 9/17/2007 pg. 4; Appellant's Response of 8/17/2007 pg. 13.

Therefore, the skilled artisan would conclude that the Office's interpretation of *transition location signal* to include the timing difference signal of Staszewski '693 is inconsistent with both the ordinary meaning of the disputed phrase and its usage in the specification. As such, the Office's construction of the disputed term is not within the broadest reasonable interpretation, and as such cannot sustain the anticipatory rejection.

Thus, the Office has failed to substantiate evidence that Staszewski '693 discloses the *transition location signal* as recited by the language of claims 1 and 20. Accordingly, Appellant respectfully requests that the Board reverse the final rejection of claims 1 and 20 and the claims depending therefrom.

THE OFFICE HAS FAILED TO SUBSTANTIATE ANTICIPATION OF CLAIM 10 BY NOT SHOWING EVIDENCE THAT STASZEWSKI '693 DISCLOSES THE *ENCODING CIRCUITRY* RECITED BY THAT CLAIM

Independent claim 10 recites in pertinent part:

> *wherein the phase/frequency comparator includes…*
> *encoding circuitry coupled to the phase detecting stage.*
> (excerpt of claim 10, emphasis added)

In support of the rejection the Office relies on the extrinsic evidence of a dictionary definition for "encoder: A digital device for converting an input digital signal into its equivalent binary code."[18] The Office's rationale for the rejection is that the NORM circuit of Staszewski '693 anticipates the *encoding circuitry* of claim 10 because it "converts the input digital signal into its equivalent binary code," repeatedly citing the following passage of Staszewski '693 in support of that position:[19]

> Moving now to FIG. 2, a simple block diagram illustrates a digital fractional phase detector system 200 according to

[18] Office Action of 2/28/2006 pg. 8.
[19] Office Action of 5/17/2007 pg. 7; Office Action of 2/28/2006 pg. 8.

one embodiment of the present invention. The system 200 is capable of accommodating a quantization scheme to measure fractional (sub-T_v) delay differences between the significant edge of the dVCO 104 clock CKV 114 and the FREF oscillator 110 reference clock 112. The system 200 uses a time-to-digital converter (TDC) 201 with a resolution of Δt_{ref} and expresses the time difference as a digital word. Due to the dVCO 104 edge counting nature of the PLL, it can be appreciated that the phase quantization resolution cannot be better than +/-π radians as stated above. A much finer phase resolution however, is required for wireless applications such as "BLUETOOTH." Such finer resolution must be achieved without forsaking the requisite digital signal processing capabilities.

FIG. 8 is a simplified schematic diagram illustrating a scheme for correcting the integer-loop quantization error $\varepsilon(k)$ by means of a fractional phase detector (PDF) 804 for the all-digital PLL synthesizer 100 shown in FIG. 1. The phase output, PHD 802, of the integer part of the PLL-loop 800, contains the fractional part of the accumulated FCW word 116, frac(θ_r), if the desired fractional division ratio FCW 116 is generally fractional-N. A preferred alternative method by which frac(θ_r) is subtracted from both the integer reference phase θ_r and the fractional correction $\varepsilon(k)$ is discussed herein below with reference to FIGS. 2-6, and is captured schematically on FIG. 1. The solution illustrated in FIG. 2 measures the one-sided fractional (sub-T_v) delay difference between the dVCO 104 clock CKV 114 and the FREF oscillator 110 clock 112 to express the time difference as a digital word ε 202. According to one embodiment, the maximum readily achievable timing resolution of the digital fractional phase detector 200 is determined by an inverter delay associated with a given CMOS process, and is about 40 psec for the C035.1 CMOS process developed by Texas Instruments Incorporated of Dallas, Tex. The digital fractional phase is determined by passing the dVCO 104 clock CKV 114 through a chain of inverters (such as shown in FIG. 5), such that each inverter output would produce a clock pulse slightly delayed from that of the immediately previous inverter. The resultant staggered clock phases would then be sampled by the same reference clock.
(Staszewski '693 col. 5 line 64 to col. 6 line 43)

The rejection is without merit because Appellant has shown that this passage on which the Office relies neither discusses the NORM circuit nor discloses anything that "converts the input digital signal into its equivalent binary code."[20] The reasoning for the rejection is based upon a misplaced characterization of the cited reference.

Furthermore, Appellant has shown that the NORM (normalization) circuit of Staszewski '693 alters the input value quantitatively, not qualitatively, and that as such the skilled artisan would readily understand that the NORM circuit of Staszewski '693 is not within the ordinary meaning of what is referred to as an "encoding circuit."[21]

Therefore, the skilled artisan would conclude that the Office's interpretation of *encoding circuit* to include the NORM of Staszewski '693 is inconsistent with both the ordinary meaning of the term and its usage in the specification. As such, the Office's construction of the disputed term is not within the broadest reasonable interpretation, and as such cannot sustain the anticipatory rejection.

Accordingly, Appellant respectfully requests that the Board reverse the rejection of claim 10 and the claims depending therefrom.

Conclusion

In conclusion, Appellant has respectfully requested that the Board reverse the rejection of all claims on appeal.

Respectfully submitted,

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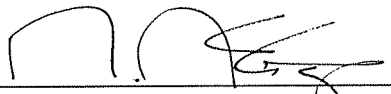
[20] Appellant's Pre-Brief Request of 9/17/2007 pg. 5; Appellant's Response of 8/17/2007 pg. 14-15; Appellant's Response of 2/14/2007 ppg. 11-13; Appellant's Response of 5/30/2006 ppg. 14-17; Appellant's Response of 11/28/2005 ppg. 18-20.

[21] *Id.*

By: 

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VIII. CLAIMS APPENDIX

1. (Previously presented) An apparatus comprising a phase/frequency comparator circuit that is configured to generate a phase error responsive to a transition location signal.

2. (Previously presented) The phase/frequency comparator of claim 7, wherein the phase detecting stage further comprises:

a tapped delay line having a plurality of outputs and configured to receive a first signal; and

a parallel latch coupled to the plurality of outputs of the tapped delay line and configured to receive a second signal,

wherein the parallel latch stores the values of the plurality of outputs of the tapped delay line in response to a transition in the second signal; and

wherein the encoding circuitry converts the values stored in the parallel latch into the numerical phase difference value.

3. (Previously presented) The phase/frequency comparator of claim 2, further comprising:

an accumulator coupled to the encoding circuitry,

wherein the accumulator adds the numerical phase difference value to a value stored in the accumulator to obtain an accumulated phase error.

4. (Previously presented) The phase/frequency comparator of claim 3, wherein the encoding circuitry includes:

an edge detector coupled to the parallel latch; and

a weighted encoder,

wherein the edge detector outputs a transition location signal that indicates a location of a transition in the values stored in the parallel latch; and

wherein the weighted encoder outputs a weighted numerical value that corresponds to the transition location signal.

5. (Previously presented) The phase/frequency comparator of claim 4, wherein the encoding circuitry includes:

a phase difference calculator configured to receive a lockpoint input,

wherein the phase difference calculator calculates a signed difference between the weighted numerical value and the lockpoint input; and

wherein the signed difference is presented to the accumulator as the numerical phase difference value.

6. (Previously presented) The phase/frequency comparator of claim 4, wherein the weighted numerical value is presented to the accumulator as the numerical phase difference value.

7. (Previously presented) The phase/frequency comparator of claim 1 further comprising:

a phase detecting stage that generates a result that represents an instantaneous phase difference; and

encoding circuitry coupled to the phase detecting stage;

wherein the encoding circuitry converts a result of the phase detecting stage into a numerical phase difference value and outputs the transition location signal.

8. (Previously presented) The phase/frequency comparator of claim 1, wherein the phase/frequency comparator is implemented as an integrated circuit.

9. (Previously presented) The phase/frequency comparator of claim 1, wherein the phase/frequency comparator is implemented as a field-programmable gate array .

10. (Previously presented) A phase locked loop comprising:

a controllable oscillator; and

a phase/frequency comparator coupled to the controllable oscillator such that an output of the controllable oscillator is connected in a feedback loop to an input of the phase/frequency comparator and an output of the phase/frequency comparator is connected through a forward path to a control input of the controlled oscillator,

wherein the phase/frequency comparator includes:

a phase detecting stage;

encoding circuitry coupled to the phase detecting stage; and

an accumulator coupled to the encoding circuitry.

11. (Original) The phase locked loop of claim 10, wherein the phase detecting stage further comprises:

a tapped delay line having a plurality of outputs and configured to receive a first signal; and

a parallel latch coupled to the plurality of outputs of the tapped delay line and configured to receive a second signal,

wherein the parallel latch stores the values of the plurality of outputs of the tapped delay line in response to a transition in the second signal; and

wherein the encoding circuitry converts the values stored in the parallel latch into a numerical phase difference value

12. (Original) The phase locked loop of claim 11, further comprising:

an accumulator coupled to the encoding circuitry,

wherein the accumulator adds the numerical phase difference value to a value stored in the accumulator to obtain an accumulated phase error.

13. (Original) The phase locked loop of claim 12, wherein the encoding circuitry includes:

an edge detector coupled to the parallel latch; and

a weighted encoder,

wherein the edge detector outputs a transition location signal that indicates a location of a transition in the values stored in the parallel latch; and

wherein the weighted encoder outputs a weighted numerical value that corresponds to the transition location signal.

14. (Original) The phase locked loop of claim 13, wherein the encoding circuitry includes:

a phase difference calculator configured to receive a lockpoint input,

wherein the phase difference calculator calculates a signed difference between the weighted numerical value and the lockpoint input; and

wherein the signed difference is presented to the accumulator as the numerical phase difference value.

15. (Original) The phase locked loop of claim 13, wherein the weighted numerical value is presented to the accumulator as the numerical phase difference value.

16. (Original) The phase locked loop of claim 10, wherein the forward path includes additional control circuitry.

17. (Original) The phase locked loop of claim 10, wherein the controlled oscillator is a numerically controlled oscillator.

18. (Previously presented) The phase locked loop of claim 10, wherein the phase locked loop is implemented as a single monolithic integrated circuit.

19. (Previously presented) The phase locked loop of claim 10, wherein the phase locked loop is implemented as a field-programmable gate array .

20. (Previously presented) A method comprising:

generating a snapshot of a first signal in response to receiving a second signal; and

mapping the snapshot to a numerical phase difference value that is generated responsive to a signal that corresponds to a transition location of the first signal.

21. (Original) The method of claim 20, further comprising:

combining the numerical phase difference value with a value in an accumulator to obtain a new accumulator value; and

presenting the new accumulator value as a result of a phase comparison.

22. (Original) The method of claim 21, further comprising:

propagating the first signal through a tapped delay line;

latching outputs of the tapped delay line in a parallel latch in response to a transition in the second signal to obtain the snapshot of the first signal.

23. (Original) The method of claim 20, further comprising:

detecting a location of an edge in the snapshot of the first signal; and

mapping the location into a weighted numerical value.

24. (Original) The method of claim 23, further comprising:

comparing the weighted numerical value with a desired phase difference; and

presenting a difference between the weighted numerical value and the desired phase difference as the numerical phase difference value.

25. (Original) The method of claim 20, further comprising:

controlling an output frequency of an oscillator using the result of the phase comparison.

26. (Original) The method of claim 25, wherein one of the first signal and the second signal is an output of the oscillator.

IX. EVIDENCE APPENDIX

No additional evidence is included.

X. RELATED PROCEEDINGS APPENDIX

There exist no relevant related proceedings concerning this Appeal before the Board.